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EXAMINER	
GARCIA OTERO, EDUARDO	

ART UNIT	PAPER NUMBER
2123	18

DATE MAILED: 01/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/360,069	WOHL ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION: Non-Final

Introduction

1. Title is: METHOD AND SYSTEM FOR GENERATING AN ATPG MODEL OF A MEMORY FROM BEHAVIORAL DESCRIPTIONS

2. First named inventor is: WOHL

3. This action is in reply to Applicant's Request for Continued Examination and Amendment received 11/28/03.

4. Claims 1-36 are cancelled, and claims 37-58 are added.

5. This is the first office action after the second Request for Continued Examination.

Index of Prior Art and Dictionaries

6. **Cheng** refers to Gate-Level Test Generation for Sequential Circuits, by Kwang-Ting Cheng, ACM Transactions on Design Automation of Electronic Systems, Vol. 1, No. 4, October 1996, Pages 405-442.

7. **Beausang'771** refers to US Patent 5,696,771.

8. **"Using Verilog Simulation Libraries for ATPG"** refers to "Using Verilog Simulation Libraries for ATPG", 0-7803-5753-1/99 1999 IEEE, by Peter Wohl, and John Waicukauski (102a type prior art, and different inventive entity than present application).

9. **Tucker** refers to "The Computer Science and Engineering Handbook", by Allen B. Tucker, CRC Press, ISBN: 0-8493-2909-4, 1996, pages 450-453.

10. **Smith** refers to "HDL Chip Design" by Douglas J. Smith, 1996, Ninth printing 2001 minor updates, ISBN 0-9651934-3-8, pages 38-40.

11. **MS Dictionary** refers to Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999.

12. **McGraw-Hill Dictionary** refers to The McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition, by McGraw-Hill Companies, Inc., 2003, ISBN 0-07-042313-X.

13. **IEEE Dictionary** refers to The Authoritative Dictionary of IEEE Standards and Terms, Seventh Edition, by IEEE Press, ISBN 0-7381-2601-2, 2000.

Applicant's Remarks

14. PRIOR ART. Applicant discusses new claim 37 in detail, and asserts that new claim 37 is not disclosed by the prior art previously used to reject cancelled claims 1-36. The Examiner has kept this discussion in mind while examining the new claims.

Definitions

15. **"Primitive"** is defined as "[COMPUT SCI] A sketchy specification, omitting details, of some action in a computer program", by McGraw-Hill Dictionary.

16. **"Primitive"** is defined as "In programming, a fundamental element in a language that can be used to create larger procedures that do the work a programmer wants", by MS Dictionary.

17. **"Logical"** is defined as "Based on true and false alternatives as opposed to arithmetic calculation of numeric values... Boolean algebra", by MS Dictionary.

18. **"Automatic test pattern generator (ATPG)"** as "Any tool that generates test information for a device based on structural analysis of the device", by IEEE Dictionary.

19. "**Content addressable memory**" (CAM) is defined as "See: associative memory" by IEEE Dictionary.

20. **"Associative memory"** is defined as "A type of memory whose locations are identified by their contents or by a part of their contents, rather than by their names or positions. Synonyms: search memory, content addressable storage" by IEEE Dictionary. Note that Tucker page 450-453 states "The cache memory is associative, or content-addressable. In an associative memory, the address of a memory location is stored, along with its content. Rather than reading data directly from a memory location, the cache is given an address and responds by providing data which may or may not be the data requested. When a cache miss occurs, the memory access is then performed with respect to the backing storage, and the cache is updated to include the new data."

21. **"Random access memory (RAM)"** is defined as "(1) A memory that permits access to any of its address locations in any desired sequence with similar access time to each location (adapted from IEC 748-2). Note: The term RAM, as commonly used, denotes a read/write memory with unlimited data rewrite capability and equal read and write times." by IEEE Dictionary.

35 USC § 101-statutory subject matter

22. 35 U.S.C. 101 reads as follows: Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

23. **Claims 37-58 are rejected under 35 U.S.C. 101** because the claimed invention is directed to non-statutory subject matter. Specifically, the claims are directed towards "memory models" without producing "useful, concrete, and tangible" results as required by *In re Alappat*, 33 F.3d 1524, 1544, 31 USPQ2d 1545, 1557 (Fed. Cir. 1994).

24. An additional limitation in the independent claims using the created model for a "useful, concrete, and tangible" purpose may satisfy the requirements of 35 USC 101. See MPEP 2106(II)(A)

25. Additionally, note *In re Sarker*, 200 USPQ 132, (CCPA), Dec. 7 1978 at page 137 discusses the significance of "post-solution activity" like building a bridge or a dam, and states "While it is true that the final step in each of these claims makes reference to the mathematical result achieved by performing the prior recited steps, we consider the connection to be so tenuous that the several steps recited in each claim when considered as a whole do not constitute a proper method under the statute".

Claim Rejections - 35 USC § 102(f)

26. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless – (f) he did not himself invent the subject matter sought to be patented.

27. There is reason to question the list of inventors in the present application. Specifically, the publication "Using Verilog Simulation Libraries for ATPG", 0-7803-5753-1/99 1999 IEEE, is co-authored by Peter Wohl, and John Waicukauski. The present application lists three inventors: Peter Wohl, John Waicukauski, and Timothy G. Hunkler. Note that Timothy G. Hunkler is not a co-author of said publication.

28. Thus, all of the present claims appear to be disclosed by said paper, as discussed in the 35 USC 102(a) rejections below.

35 USC § 112- first paragraph- enablement

29. The following is a quotation of the first paragraph of 35 U.S.C. 112: The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

30. **Claims 37-58 are rejected under 35 U.S.C. 112, first paragraph,** as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

31. In claim 37, the relationship between the 5 limitations is not clear. First, the claim terminology "for coupling" is interpreted as mere intended use. Second, even if "for coupling to..." is interpreted as "coupled to...", the overall functional relationship is not clear.

32. In claim 37, as written, the "memory primitive" is coupled to the "address bus primitive", which is coupled to the "read data port primitive" which is coupled to the "output port of the memory primitive". Note that the coupling appears to be in a feedback/circular loop. This claimed feedback/circular arrangement is not reflected in FIG 6A, nor in FIG 7A-C. Further, it is not clear whether the term "output port of the memory primitive" in the second limitation is intended as a part of said "memory primitive", or as a separate entity. Additionally, note that coupling in logic circuits is generally assumed to be uni-directional, and "A coupled to B" means that the signal(s) flow from A to B.

33. It is possible that the Applicant is attempting to claim the configuration of FIG 7 in "Using Verilog Simulation Libraries for ATPG", but this is not clear.

34. Claims 38-58 are similarly rejected.

35 USC § 112-Second Paragraph-indefinite claims

35. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

36. **Claims 37-58 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

37. In claim 37, the relationship between the 5 limitations is not clear. First, the claim terminology "for coupling" is interpreted as mere intended use. Second, even if "for coupling to..." is interpreted as "coupled to...", the overall functional relationship is not clear.

38. In claim 37, as written, the "memory primitive" is coupled to the "address bus primitive", which is coupled to the "read data port primitive" which is coupled to the "output port of the memory primitive". Note that the coupling appears to be in a feedback/circular loop. This claimed feedback/circular arrangement is not reflected in FIG 6A, nor in FIG 7A-C. Further, it is not clear whether the term "output port of the memory primitive" in the second limitation is intended as a part of said "memory primitive", or as a separate entity. Additionally, note that coupling in logic circuits is generally assumed to be uni-directional, and "A coupled to B" means that the signal(s) flow from A to B.

39. It is possible that the Applicant is attempting to claim the configuration of FIG 7 in "Using Verilog Simulation Libraries for ATPG", but this is not clear.

40. Claims 38-58 are similarly rejected.

Drawings-additional drawings required

41. "The applicant shall furnish a drawing where necessary for the understanding of the subject matter to be patented" 35 USC 113. Applicant is required to furnish a drawing under 37 CFR 1.81. No new matter may be introduced in the required drawing.

42. Specifically, the Examiner requires a drawing showing the elements, and the relationship between the elements of Claim 37, 51, 53, and 55 (all the independent claims). In view of the above 35 USC 112 rejections, additional drawings are necessary to understand the subject matter to be patented.

43. For example, claim 37 appears to be 5 types of elements in 5 limitations: "a memory primitive", "a read data port primitive", "an address bus primitive", "a data bus primitive", and "a plurality of memory out primitives". However, the claim 37 coupling between these elements is ambiguous. The Examiner drew a layout based on claim 37, and said drawing did not match FIG 7 in "Using Verilog Simulation Libraries for ATPG". However, it appears that Applicant's intent is that claim 37 should represent FIG 7 in "Using Verilog Simulation Libraries for ATPG". Said FIG 7 is not part of the specification (but is part of an Information Disclosure Statement).

44. It will be greatly accelerate the prosecution of this application if drawings supported the independent claims. The Examiner invites a telephone interview, and perhaps the number of drawings may be minimized.

Claim Interpretation

45. In claim 37 (and throughout the claims), the term **"for coupling"** is interpreted merely as an intended use.

46. In claim 53, the preamble term **"combined content addressable memory (CAM) and random access memory (RAM)"** is interpreted as merely intended use.

Claim Rejections - 35 USC § 102(a)

47. The following is a quotation of 35 U.S.C. 102(a) which forms the basis for the rejections under this section in this Office action: (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

48. Claims 37-58 are rejected under 35 U.S.C. 102(a).

49. Claim 37 is rejected under 35 U.S.C. 102(a) as being anticipated by "Using Verilog Simulation Libraries for ATPG".

50. Claim 37 is an independent "memory model" claim with 5 limitations, labeled by the Examiner.

[1] **"a memory primitive"**

[2] **"a read data port primitive"**

[3] **"an address bus primitive** for coupling to the memory primitive and the read data port primitive"

[4] **"a data bus primitive** for coupling to the memory primitive"

[5] **"a plurality of memory out primitives,** each memory out primitive for coupling to the read data port primitive"

51. Limitations [1] through [5] are disclosed by Figure 7 "ATPG model of the RAM in Figure 6" at page 1017 of "Using Verilog Simulation Libraries for ATPG".

52. Claims 38-50 are rejected under 35 U.S.C. 102(a) as being anticipated by "Using Verilog Simulation Libraries for ATPG".

53. Claims 38-50 depend from independent claim 37.

54. In claim 38, there are 7 limitations:

[1] **"a set input port"**

[2] **"a reset port"**

[3] **"a write_clock port"**

[4] **"a write_enable port"**

[5] **"a write_address port** for coupling to an output of the address bus primitive"

[6] **"a write_data port** for coupling to an output of the data bus primitive"

[7] **"an output port"**

55. Limitations [1] through [7] are disclosed by Figure 7 "ATPG model of the RAM in Figure 6" at page 1017 of under 35 U.S.C. 102(a) as being anticipated by "Using Verilog Simulation Libraries for ATPG".

56. In claim 39, "the read data port primitive represents a **read port functionality of the memory**" is disclosed by Figure 7 "ATPG model of the RAM in Figure 6" at page 1017 of "Using Verilog Simulation Libraries for ATPG". Also see page 1017 section 5.5.5. "RPORT (Read Port)".

57. In claim 40, there are 4 limitations:

[1] "the read data port primitive includes: **a read enable port"**

[2] "a read_address port for coupling to the address bus primitive"

[3] "a read_data port for coupling to the memory primitive"

[4] "an output port for coupling to the plurality of memory out primitives, wherein a dimension of the output port corresponds to a data dimension of the memory primitive"

58. Limitations [1] to [4] are disclosed by Figure 7 "ATPG model of the RAM in Figure 6" at page 1017 of "Using Verilog Simulation Libraries for ATPG". Also see page 1017 section 5.5.5. "RPORT (Read Port)".

59. In claim 41 "the address bus primitive represents **an address functionality of a memory"** is disclosed by Figure 7 "ATPG model of the RAM in Figure 6" at page 1017 of "Using Verilog Simulation Libraries for ATPG". Also see page 1019 Section 5.8 "Same-Address Contention".

60. In claim 42, there are 2 limitations:

[1] "the address bus primitive includes: **a plurality of input ports corresponding to an address dimension** of the memory primitive"

[2] "[the address bus primitive includes:]... **an output port for coupling to the memory primitive and the read data port primitive**"

61. Limitations [1] and [2] are disclosed by disclosed by Figure 7 "ATPG model of the RAM in Figure 6" at page 1017 of "Using Verilog Simulation Libraries for ATPG". Also see page 1019 Section 5.8 "Same-Address Contention".

62. In claim 43, "**the address bus primitive** further includes an attribute indicating whether an incoming address is encoded or decoded" is disclosed by disclosed by Figure 7 "ATPG model of the RAM in Figure 6" at page 1017 of "Using Verilog Simulation Libraries for ATPG". Also see page 1019 Section 5.8 "Same-Address Contention".

63. In claim 44, "the data bus primitive represents **a data bus functionality of the memory**" is disclosed by Figure 7 "ATPG model of the RAM in Figure 6" at page 1017 of "Using Verilog Simulation Libraries for ATPG". Also see page 1017 section 5.4.3 "DATABUS (Data Bus)".

64. In claim 45, there are 2 limitations:

[1] **"a plurality of input ports** corresponding to a data dimension of the memory primitive"

[2] **"an output port** for coupling to the memory primitive"

65. Limitations [1] and [2] are disclosed by disclosed by Figure 7 "ATPG model of the RAM in Figure 6" at page 1017 of "Using Verilog Simulation Libraries for ATPG".

66. In claim 46, **"each memory out primitive represents a simulated value storage functionality of the memory"** is disclosed by Figure 7 "ATPG model of the RAM in Figure 6" at page 1017 of "Using Verilog Simulation Libraries for ATPG". Also see page 1017 section 5.4.3 "DATABUS (Data Bus)".

67. In claim 47, there are two limitations:

[1] **"each memory out primitive includes: an input port"**

[2] "[each memory out primitive includes:]... **an output port"**

68. Limitations [1] and [2] are disclosed by disclosed by Figure 7 "ATPG model of the RAM in Figure 6" at page 1017 of "Using Verilog Simulation Libraries for ATPG".

69. In claim 48, **"a plurality of tristate drivers** can be coupled to output ports of the memory out primitives, thereby representing an attribute of the read data port primitive" is disclosed by "Using Verilog Simulation Libraries for ATPG" at page 8 "Collapsing the eight

strengths of Verilog into three levels for ATPG provides a very efficient model". Also see FIG 3 at page 1014.

70. In claim 49, "a plurality of edge-triggered registers can be coupled to the output ports of the memory primitives, thereby representing an attribute of the read data port primitive" is disclosed by "edge-triggered" at page 1017 of "Using Verilog Simulation Libraries for ATPG". Also see page 1019 "level and edge sensitive reads".

71. In claim 50, "a plurality of tristate drivers can be coupled to the output ports of the plurality of edge-triggered registers, thereby representing an attribute of the read data port primitive" is disclosed by "Using Verilog Simulation Libraries for ATPG" at page 1018 section 5.7.2 "tri-state drivers". Also see page 1013 "Collapsing the eight strengths of Verilog into three levels for ATPG provides a very efficient model". Also see FIG 3 at page 1014. Also see page 1019 "level and edge sensitive reads".

72. **Claim 51 is rejected** under 35 U.S.C. 102(a) as being anticipated by "Using Verilog Simulation Libraries for ATPG".

73. Claim 51 is an independent "model" claim with 5 limitations, labeled by the Examiner.

[1] **"a memory primitive"**

[2] **"compare port primitive** for coupling to an output port of the memory primitive"

[3] **"an address bus primitive** for coupling to the memory primitive and the compare port primitive"

[4] **"a data bus primitive** for coupling to the memory primitive"

[5] **"a plurality of memory out primitives,** each memory out primitive for coupling to the compare port primitive"

74. Limitations [1] through [5] are disclosed by "Using Verilog Simulation Libraries for ATPG" at Figure 9 page 1018, and Figure 7 "ATPG model of the RAM in Figure 6" at page 1017. Note that one of ordinary skill in the art would be very familiar with CAM (content addressable memory) as a form of RAM (random access memory) typically used in microprocessor caches, and thus would interpret said Figure 7 broadly as disclosing similar ATPG models for CAM, including compare ports which are an essential part of CAM.

75. **Claim 52 is rejected** under 35 U.S.C. 102(a) as being anticipated by "Using Verilog Simulation Libraries for ATPG".

76. Claim 52 depends from claim 51, with 4 additional limitations:

[1] "the compare port primitive includes: a compare enable port"

[2] "[the compare port primitive includes:]... a data bus port for coupling to an output port of the data bus primitive"

[3] "[the compare port primitive includes:]... a data bus port for coupling to an output port of the memory primitive"

[4] "[the compare port primitive includes:]... a data port for coupling to input ports of the plurality of memory output primitives"

77. Limitations [1] through [4] are disclosed by "Using Verilog Simulation Libraries for ATPG" at Figure 9 page 1018, and Figure 7 "ATPG model of the RAM in Figure 6" at page 1017. Note that one of ordinary skill in the art would be very familiar with CAM (content addressable memory) as a form of RAM (random access memory) typically used in microprocessor caches, and thus would interpret said Figure 7 broadly as disclosing similar ATPG models for CAM, including compare ports which are an essential part of CAM.

78. **Claim 53 is rejected** under 35 U.S.C. 102(a) as being anticipated by "Using Verilog Simulation Libraries for ATPG".

79. Claim 53 is an independent "model" claim with 8 limitations.

[1] "a first memory primitive"

[2] "a data bus primitive"

[3] "a compare port primitive for coupling to the memory primitive and the data bus primitive"

[4] "a plurality of memory output primitives, each memory output primitive for coupling to the read data port primitive"

[5] "an address bus primitive for coupling to a first subset of the plurality of memory output primitives"

[6] "a second memory primitive"

[7] "a read data port primitive for coupling to the second memory primitive, the address bus primitive, and a second subset of the plurality of memory output primitives" is

[8] "a plurality of memory output primitives, each memory output primitive for coupling to the read data port primitive"

80. Limitations [1] through [8] are disclosed by "Using Verilog Simulation Libraries for ATPG" at page 1018 Figure 9, and page 1017 Figure 7. Note that one of ordinary skill in the art would be very familiar with CAM (content addressable memory) as a form of RAM (random access memory) typically used in microprocessor caches, and thus would interpret said Figure 7 broadly as disclosing similar ATPG models for CAM, including compare ports which are an essential part of CAM.

81. **Claim 54 is rejected** under 35 U.S.C. 102(a) as being anticipated by "Using Verilog Simulation Libraries for ATPG".

82. Claim 54 depends from claim 53, with 4 additional limitations:

[1] "a compare enable port"

[2] "a data bus port for coupling to an output port of the data bus primitive"

[3] "a data port for coupling to an output port of the memory primitive"

[4] "an output port for coupling to input ports of the plurality of memory output primitives"

83. Limitations [1] through [4] are disclosed by "Using Verilog Simulation Libraries for ATPG" at page 1018 Figure 9, and page 1017 Figure 7. Note that one of ordinary skill in the art would be very familiar with CAM (content addressable memory) as a form of RAM (random access memory) typically used in microprocessor caches, and thus would interpret said Figure 7 broadly as disclosing similar ATPG models for CAM, including compare ports which are an essential part of CAM.

84. **Claim 55 is rejected** under 35 U.S.C. 102(a) as being anticipated by "Using Verilog Simulation Libraries for ATPG".

85. Claim 55 is an independent "model" claim with 1 limitation: [1] "a plurality of primitives, each primitive representing a defined functionality of a memory" is disclosed by "Using Verilog Simulation Libraries for ATPG" at page 1018 Figure 9, and page 1017 Figure 7. Note that one of ordinary skill in the art would be very familiar with CAM (content addressable memory) as a form of RAM (random access memory) typically used in microprocessor caches, and thus would interpret said Figure 7 broadly as disclosing similar ATPG models for CAM, including compare ports which are an essential part of CAM.

86. **Claims 56-58 are rejected** under 35 U.S.C. 102(a) as being anticipated by "Using Verilog Simulation Libraries for ATPG".

87. Claim 56-58 depend from independent claim 55.

88. In claim 56, "each primitive usable by the ATPG tool is configured based on a subset of behavioral hardware description language (HDL) usable by the simulation tool" is disclosed by "Using Verilog Simulation Libraries for ATPG" at page 1013 section 3.4 "Timing only Circuitry" and "eliminate unused circuitry".

89. In claim 57, "the behavioral HDL includes Verilog" is disclosed by "Using Verilog Simulation Libraries for ATPG" at page 1011 "Verilog language".

90. In claim 58, "the subset of behavioral HDL can directly map to the plurality of primitives" is disclosed by "Using Verilog Simulation Libraries for ATPG", page 1011 Figure 2.

Additional Cited Prior Art

91. The following US patents or publications are hereby cited as prior art, but have not been used for rejection. Applicant should review these carefully before responding to this office action.

92. The Computer Science and Engineering Handbook, by Allen B. Tucker, CRC Press, ISBN: 0-8493-2909-4, 1996, pages 450-453, discloses "The cache memory is associative, or content-addressable. In an associative memory, the address of a memory location is stored, along with its content. Rather than reading data directly from a memory location, the cache is given an address and responds by providing data which may or may not be the data requested. When a cache miss occurs, the memory access is then performed with respect to the backing storage, and the cache is updated to include the new data."

93. "HDL Chip Design" by Douglas J. Smith, 1996, Ninth printing 2001 minor updates, ISBN 0-9651934-3-8, pages 38-4, discloses "partition the design into natural abstract blocks known as components. Each component is the instantiation of a design entity, which is normally modeled in a separate system file for easy management and individual compilation by simulation or synthesis tools". Thus, Smith's "component" appears equivalent to a "primitive" in the present application.

Conclusion

94. All claims stand rejected under 35 USC 101, 35 USC 102(a), and 35 USC 102(f), and 35 USC 112. Further, additional drawings are required.

95. In view of the large number of issues outstanding, the Examiner suggests that a telephone interview may efficiently accelerate the prosecution of the case, and perhaps resolve some of the outstanding issues, and minimize the number of required drawings.

Communication

96. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Tuesday through Friday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for this group is 703-872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

* * * *

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100